

October 1987 Revised January 2004

#### MM74C73

### **Dual J-K Flip-Flops with Clear and Preset**

#### **General Description**

The MM74C73 dual J-K flip-flops are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement transistors. Each flip-flop has independent J, K, clock and clear inputs and Q and Q outputs. This flip-flop is edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Clear or preset is independent of the clock and is accomplished by a low level on the respective input.

#### **Features**

■ Supply voltage range: 3V to 15V

■ Tenth power TTL compatible: Drive 2 LPTTL loads

■ High noise immunity: 0.45 V<sub>CC</sub> (typ.)

■ Low power: 50 nW (typ.)

■ Medium speed operation: 10 MHz (typ.)

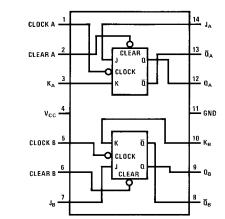
#### **Applications**

- Automotive
- · Data terminals
- Instrumentation
- · Medical electronics
- Alarm systems
- · Industrial electronics
- · Remote metering
- Computers

#### **Ordering Code:**

Order Number Package Number Package Descri		Package Number	Package Description		
	MM74C73N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide		

#### **Connection Diagram**



Note: A logic "0" on clear sets Q to logic "0".

**Top View** 

#### **Truth Table**

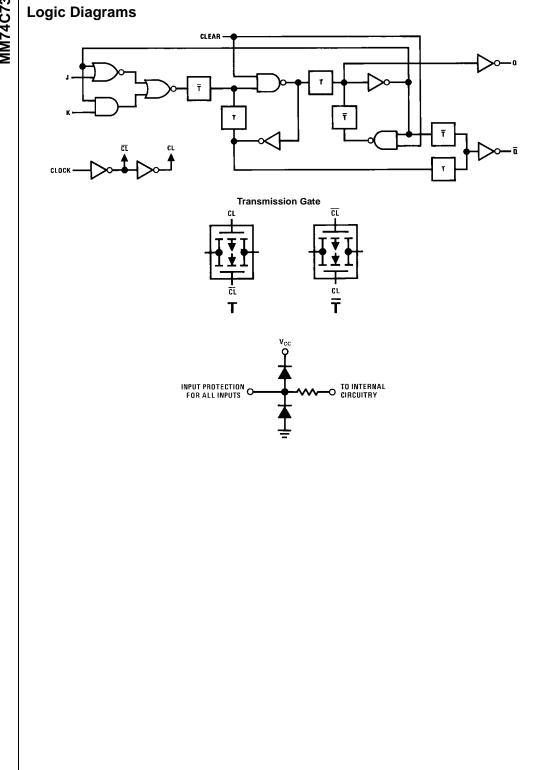
	t <sub>n</sub>	
J	K	Q
0	0	$Q_n$
0	1	0
1	0	1
1	1	$\overline{Q}_n$

Preset		Clear	$Q_n$	$\overline{Q}_n$
	0	0	0	0
	0	1	1	0
	1	0	0	1
	1	1	$Q_n$	$\overline{Q}_n$
			(Note 1)	(Note 1)

t<sub>n</sub> = bit time before clock pulse

t<sub>n+1</sub> = bit time after clock pulse

Note 1: No change in output from previous state



#### Absolute Maximum Ratings(Note 2)

 $\begin{array}{lll} \mbox{Voltage at Any Pin} & -0.3\mbox{V to V}_{\mbox{CC}} + 0.3\mbox{V} \\ \mbox{Operating Temperature Range} & -55\mbox{°C to } +125\mbox{°C} \\ \mbox{Storage Temperature} & -65\mbox{°C to } +150\mbox{°C} \\ \end{array}$ 

Power Dissipation

Dual-In-Line 700 mW

Small Outline 500 mW

Lead Temperature

(Soldering, 10 seconds) 260°C

Operating  $V_{CC}$  Range +3V to 15V

V<sub>CC</sub> (Max) 18V

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of Electrical Characteristics provides conditions for actual device operation.

#### **DC Electrical Characteristics**

Min/Max limits apply across temperature range unless otherwise noted

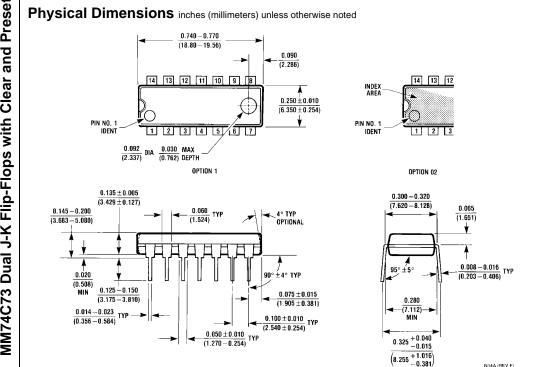
Symbol	Parameter	Conditions	Min	Тур	Max	Units
CMOS TO	CMOS		•		•	-
V <sub>IN(1)</sub>	Logical "1" Input Voltage	V <sub>CC</sub> = 5V	3.5			V
		V <sub>CC</sub> = 10V	8			
V <sub>IN(0)</sub>	Logical "0" Input Voltage	V <sub>CC</sub> = 5V			1.5	V
		V <sub>CC</sub> = 10V			2	
V <sub>OUT(1)</sub>	Logical "1" Output Voltage	V <sub>CC</sub> = 5V	4.5			V
		V <sub>CC</sub> = 10V	9			1
V <sub>OUT(0)</sub>	Logical "0" Output Voltage	V <sub>CC</sub> = 5V			0.5	V
		V <sub>CC</sub> = 10V			1	v
I <sub>IN(1)</sub>	Logical "1" Input Current	V <sub>CC</sub> = 15V			1	μΑ
I <sub>IN(0)</sub>	Logical "0" Input Current	V <sub>CC</sub> = 15V	-1			μΑ
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = 15V		0.050	60	μΑ
LOW POW	ER TTL TO CMOS INTERFACE					
V <sub>IN(1)</sub>	Logical "1" Input Voltage	V <sub>CC</sub> = 4.75V	V <sub>CC</sub> – 1.5			V
V <sub>IN(0)</sub>	Logical "0" Input Voltage	V <sub>CC</sub> = 4.75V			0.8	V
V <sub>OUT(1)</sub>	Logical "1" Output Voltage	$V_{CC} = 4.75V$ , $I_{O} = -360 \mu A$	2.4			V
V <sub>OUT(0)</sub>	Logical "0" Output Voltage	$V_{CC} = 4.75V$ , $I_{O} = 360 \mu A$			0.4	V
OUTPUT D	RIVE (See Family Characteristics	Data Sheet) (Short Circuit Current)				
I <sub>SOURCE</sub>	Output Source Current	$V_{CC} = 5V, V_{IN(0)} = 0V$	-1.75			mA
		$T_A = 25$ °C, $V_{OUT} = 0$ V	-1.73			
I <sub>SOURCE</sub>	Output Source Current	$V_{CC} = 10V, V_{IN(0)} = 0V$	-8			mA
		$T_A = 25$ °C, $V_{OUT} = 0V$	-6			
I <sub>SINK</sub>	Output Sink Current	$V_{CC} = 5V, V_{IN(1)} = 5V$	1.75			mA
		$T_A = 25$ °C, $V_{OUT} = V_{CC}$				
I <sub>SINK</sub>	Output Sink Current	$V_{CC} = 10V, V_{IN(1)} = 10V$	8		mA	
		$T_A = 25^{\circ}C$ , $V_{OUT} = V_{CC}$				111/4

# AC Electrical Characteristics (Note 3) $T_A = 25^{\circ}\text{C}, \ C_L = 50 \ \text{pF}, \ \text{unless otherwise noted}$

Parameter	Conditions	Min	Тур	Max	Units
Input Capacitance	Any Input		5		pF
Propagation Delay Time to a	V <sub>CC</sub> = 5V		180	300	ns
Logical "0" or Logical "1" from	V <sub>CC</sub> = 10V		70	110	
Clock to Q or Q					
Propagation Delay Time to a	V <sub>CC</sub> = 5V		200	300	ns
Logical "0" from Preset or Clear	V <sub>CC</sub> = 10V		80	130	
Propagation Delay Time to a	V <sub>CC</sub> = 5V		200	300	ns
Logical "1" from Preset or Clear	$V_{CC} = 10V$		80	130	
Time Prior to Clock Pulse that	V <sub>CC</sub> = 5V		110	175	ns
Data must be Present	V <sub>CC</sub> = 10V		45	70	
Time after Clock Pulse that J	V <sub>CC</sub> = 5V		-40	0	ns
and K must be Held	V <sub>CC</sub> = 10V		-20	0	
Minimum Clock Pulse Width	V <sub>CC</sub> = 5V		120	190	ns
$t_{WL} = t_{WH}$	V <sub>CC</sub> = 10V		50	80	
Minimum Preset and Clear	V <sub>CC</sub> = 5V		90	130	ns
Pulse Width	V <sub>CC</sub> = 10V		40	60	
Maximum Toggle Frequency	V <sub>CC</sub> = 5V	2.5	4		MHz
	V <sub>CC</sub> = 10V	7	11		
Clock Pulse Rise and Fall Time	V <sub>CC</sub> = 5V			15	μs
	V <sub>CC</sub> = 10V			5	
	Input Capacitance Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q or Q  Propagation Delay Time to a Logical "0" from Preset or Clear Propagation Delay Time to a Logical "0" from Preset or Clear Propagation Delay Time to a Logical "1" from Preset or Clear Time Prior to Clock Pulse that Data must be Present Time after Clock Pulse that J and K must be Held Minimum Clock Pulse Width t <sub>WL</sub> = t <sub>WH</sub> Minimum Preset and Clear Pulse Width Maximum Toggle Frequency	Input Capacitance Any Input  Propagation Delay Time to a Logical "0" or Logical "1" from V <sub>CC</sub> = $5$ V  Logical "0" or Logical "1" from V <sub>CC</sub> = $1$ 0V  Propagation Delay Time to a Logical "0" from Preset or Clear V <sub>CC</sub> = $1$ 0V  Propagation Delay Time to a Logical "1" from Preset or Clear V <sub>CC</sub> = $1$ 0V  Propagation Delay Time to a Logical "1" from Preset or Clear V <sub>CC</sub> = $1$ 0V  Time Prior to Clock Pulse that V <sub>CC</sub> = $1$ 0V  Time Prior to Clock Pulse that V <sub>CC</sub> = $1$ 0V  Time after Clock Pulse that J And K must be Held V <sub>CC</sub> = $1$ 0V  Minimum Clock Pulse Width V <sub>CC</sub> = $1$ 0V  Minimum Preset and Clear V <sub>CC</sub> = $1$ 0V  Minimum Preset and Clear V <sub>CC</sub> = $1$ 0V  Maximum Toggle Frequency V <sub>CC</sub> = $1$ 0V  Clock Pulse Rise and Fall Time V <sub>CC</sub> = $1$ 0V	Input Capacitance	Input Capacitance Any Input 5  Propagation Delay Time to a $V_{CC} = 5V$ 180  Logical "0" or Logical "1" from $V_{CC} = 10V$ 70  Clock to Q or $\overline{Q}$ 200  Propagation Delay Time to a $V_{CC} = 10V$ 80  Propagation Delay Time to a $V_{CC} = 10V$ 80  Propagation Delay Time to a $V_{CC} = 10V$ 80  Propagation Delay Time to a $V_{CC} = 10V$ 80  Time Prior to Clock Pulse that $V_{CC} = 10V$ 80  Time Prior to Clock Pulse that $V_{CC} = 10V$ 110  Data must be Present $V_{CC} = 10V$ 45  Time after Clock Pulse that J $V_{CC} = 10V$ 70  Minimum Clock Pulse Width $V_{CC} = 10V$ 70  Minimum Preset and Clear $V_{CC} = 10V$ 70  Minimum Preset and Clear $V_{CC} = 10V$ 70  Maximum Toggle Frequency $V_{CC} = 10V$ 70  Maximum Toggle Frequency $V_{CC} = 10V$ 70  Clock Pulse Rise and Fall Time $V_{CC} = 10V$ 70  Time Rice Tolock Pulse Rise and Fall Time $V_{CC} = 10V$ 70  Time After Clock Pulse Rise and Fall Time $V_{CC} = 10V$ 70  Time After Clock Pulse Rise and Fall Time $V_{CC} = 10V$ 70  Time After Clock Pulse Rise and Fall Time $V_{CC} = 10V$ 70  Time After Clock Pulse Rise After Aft	Input Capacitance

Note 3: AC Parameters are guaranteed by DC correlated testing.

## **AC Test Circuit Switching Time Waveforms** CMOS to CMOS INPUTS t<sub>SETUP</sub> $\Omega$ or $\widetilde{\Omega}$ $t_r = t_f = 20 \text{ ns}$ **Typical Applications Ripple Binary Counters** COUNTER Enable CLOCK -Shift Registers CLOCK -Guaranteed Noise Margin as a Function of $V_{CC}$ 74C Compatibility GUARANTEED OUTPUT "1" LEVEL V<sub>OUT</sub> (1) @ INPUTS = V<sub>IN</sub> (0) 13.5 74CXX LOGIC LEVELS 4.05 GUARANTEED OUTPUT "0" LEVEL V<sub>OUT</sub> (0) @ INPUTS = V<sub>IN</sub> (1) V<sub>IN</sub> (0) 0.45 10V 15V 4.50V $v_{cc}$



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- 1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- 2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com