FAIRCHILD SEMICONDUCTOR™

October 1987
Revised January 2004

MM74C73
Dual J-K Flip-Flops with Clear and Preset

General Description

The MM74C73 dual J-K flip-flops are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement transistors. Each flip-flop has independent J, K, clock and clear inputs and Q and Q outputs. This flip-flop is edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Clear or preset is independent of the clock and is accomplished by a low level on the respective input.

Features

- Supply voltage range: 3V to 15V
- Tenth power TTL compatible: Drive 2 LPTTL loads
- High noise immunity: 0.45 V_{CC} (typ.)
- Low power: 50 nW (typ.)
- Medium speed operation: 10 MHz (typ.)

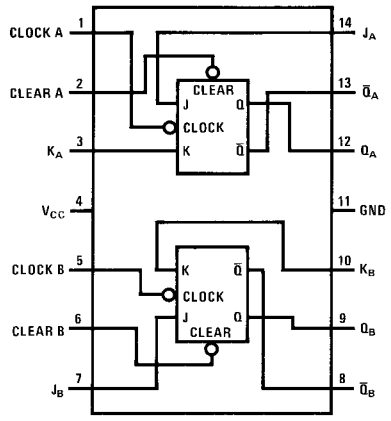
Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

Ordering Code:

Order Number	Package Number	Package Description
MM74C73N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Connection Diagram



Note: A logic "0" on clear sets Q to logic "0".

Top View

Truth Table

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

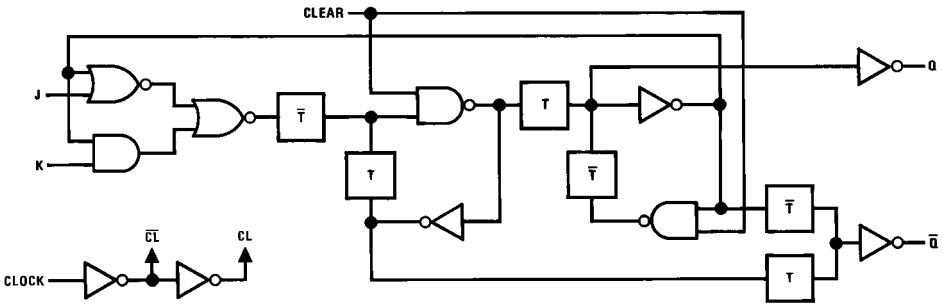
Preset	Clear	Q_n	$\overline{Q}_n$
0	0	0	0
0	1	1	0
1	0	0	1
1	1	Q_n (Note 1)	$\overline{Q}_n$ (Note 1)

t_n = bit time before clock pulse

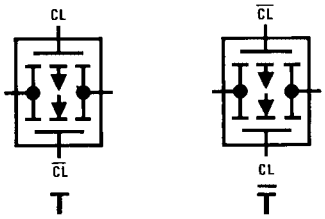
t_{n+1} = bit time after clock pulse

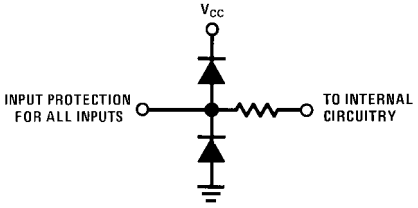
Note 1: No change in output from previous state

Logic Diagrams



Transmission Gate





Absolute Maximum Ratings(Note 2)

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature	
(Soldering, 10 seconds)	260°C
Operating V_{CC} Range	+3V to 15V
V_{CC} (Max)	18V

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of Electrical Characteristics provides conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V	3.5			V
		V_{CC} = 10V	8			
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V			1.5	V
		V_{CC} = 10V			2	
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5V	4.5			V
		V_{CC} = 10V	9			
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V			0.5	V
		V_{CC} = 10V			1	
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V			1	µA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V	−1			µA
I_{CC}	Supply Current	V_{CC} = 15V		0.050	60	µA
LOW POWER TTL TO CMOS INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 4.75V	V_{CC} − 1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 4.75V, I_O = −360 µA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 4.75V, I_O = 360 µA			0.4	V
OUTPUT DRIVE (See Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current	V_{CC} = 5V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = 0V	−1.75			mA
I_{SOURCE}	Output Source Current	V_{CC} = 10V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = 0V	−8			mA
I_{SINK}	Output Sink Current	V_{CC} = 5V, $V_{IN(1)}$ = 5V T_A = 25°C, V_{OUT} = V_{CC}	1.75			mA
I_{SINK}	Output Sink Current	V_{CC} = 10V, $V_{IN(1)}$ = 10V T_A = 25°C, V_{OUT} = V_{CC}	8			mA

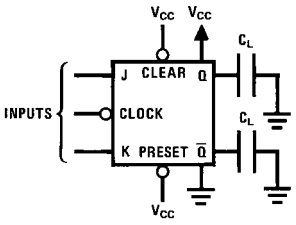
AC Electrical Characteristics (Note 3)

$T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance	Any Input		5		pF
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q or $\overline{Q}$	$V_{CC} = 5V$		180	300	ns
		$V_{CC} = 10V$		70	110	
t_{pd0}	Propagation Delay Time to a Logical "0" from Preset or Clear	$V_{CC} = 5V$		200	300	ns
		$V_{CC} = 10V$		80	130	
t_{pd}	Propagation Delay Time to a Logical "1" from Preset or Clear	$V_{CC} = 5V$		200	300	ns
		$V_{CC} = 10V$		80	130	
t_S	Time Prior to Clock Pulse that Data must be Present	$V_{CC} = 5V$		110	175	ns
		$V_{CC} = 10V$		45	70	
t_H	Time after Clock Pulse that J and K must be Held	$V_{CC} = 5V$		−40	0	ns
		$V_{CC} = 10V$		−20	0	
t_{PW}	Minimum Clock Pulse Width $t_{WL} = t_{WH}$	$V_{CC} = 5V$		120	190	ns
		$V_{CC} = 10V$		50	80	
t_{PW}	Minimum Preset and Clear Pulse Width	$V_{CC} = 5V$		90	130	ns
		$V_{CC} = 10V$		40	60	
t_{MAX}	Maximum Toggle Frequency	$V_{CC} = 5V$	2.5	4		MHz
		$V_{CC} = 10V$	7	11		
t_r, t_f	Clock Pulse Rise and Fall Time	$V_{CC} = 5V$			15	µs
		$V_{CC} = 10V$			5	

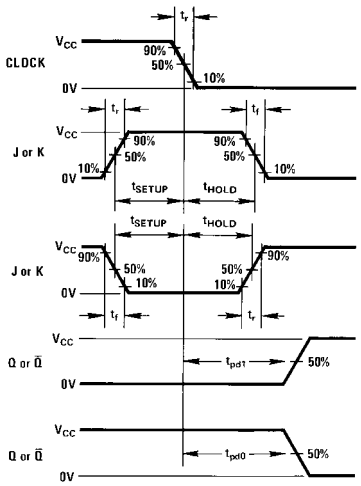
Note 3: AC Parameters are guaranteed by DC correlated testing.

AC Test Circuit



Switching Time Waveforms

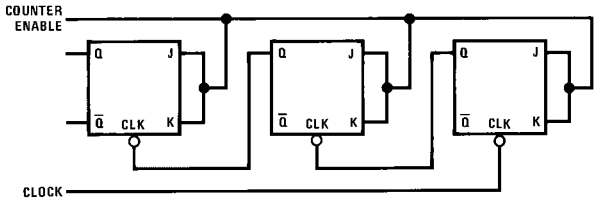
CMOS to CMOS



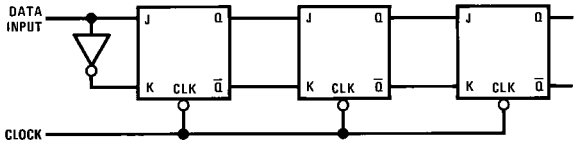
$t_r = t_f = 20$ ns

Typical Applications

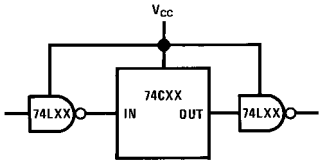
Ripple Binary Counters



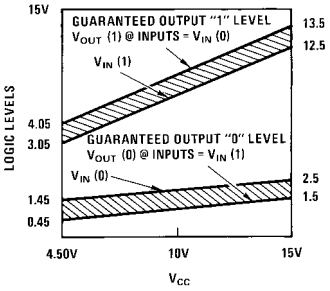
Shift Registers



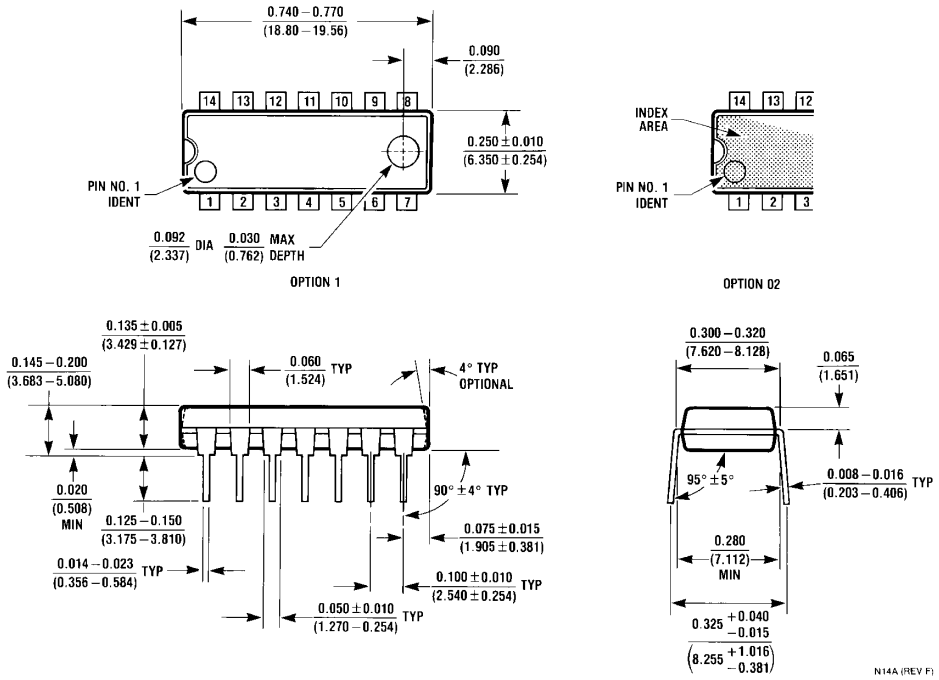
74C Compatibility



Guaranteed Noise Margin as a Function of V_{CC}



Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A